EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Robert J. Crawford (RN: 32,122) on April 08, 2010.

The application has been amended as follows:

IN THE CLAIMS

Claim 1. (Currently Amended) A lateral thin-film Silicon-On-Insulator (SOI) device comprising

a semiconductor substrate,

a buried insulating layer on said substrate, and

a lateral MOS transistor device in an SOI layer on said buried insulating layer and having

a source region of a first type conductivity formed in a body region of a second type conductivity,

a lateral drift region of a second type conductivity adjacent said body region,

a drain region of said first type conductivity and laterally spaced apart

from said body region,

a gate electrode insulated from said body region and drift region by an insulation region,

an insulation layer on and laterally adjacent to the gate electrode, and

a field plate on the insulation layer and separated from the gate electrode and the drain extension region by the insulation layer, the field plate being connected either to said source region or said gate electrode and extending substantially over said lateral drift region, wherein said field plate comprises a first layer of plural metallic regions which are isolated laterally and spaced apart from one another ~~so as to form a linear lateral electric field distribution in the lateral drift region~~ , and wherein the lateral drift region includes dopants arranged with a lateral doping gradient.

Claims 7, 14, 17 and 18. (cancelled)

Claim 8. (Currently Amended) The device of claim ~~7~~ 6 wherein said first type conductivity is p-type conductivity, and said second type conductivity is n-type conductivity.

Claim 13. (Currently Amended) A lateral thin-film Silicon-On-Insulator (SOI) device comprising

a semiconductor substrate;

a buried insulating layer on the substrate; and

a lateral MOS transistor device in an SOI layer on said buried insulating layer and having

a source region of a first conductivity type formed in a body region of a second conductivity type,

a lateral drift region of the second conductivity type adjacent the body region,

a drain region of the first conductivity type and laterally spaced apart from the body region by the lateral drift region,

a gate electrode insulated from said body region and drift region by an insulation region,

an insulation layer on and laterally adjacent to the gate electrode,

source and drain contact regions in a layer region including the gate electrode and respectively electrically contacting the source and drain regions, the contact regions being laterally separated from the gate electrode by the insulation layer and

a field plate arrangement, on the insulation layer, having a plurality of conductive regions that laterally extend substantially over the lateral drift region and that are insulated and spaced apart from one another by an insulative material, a first one of the conductive regions at a first end of the field plate being connected either to the source region or the gate electrode, the conductive regions linearly distributing a voltage at the first conductive region across the other conductive regions to an opposite end of the field plate, the distributed voltage dropping laterally across the field plate from the

first end to the opposite end, wherein the lateral drift region includes dopants arranged with a lateral doping gradient.

Claim 15. (Currently Amended) The device of claim 13, wherein ~~the field plate arrangement provides~~ a linearly- graded charge profile is provided to the lateral drift region, the charge profile dropping linearly from a high charge profile below the first end of the field plate arrangement to a low charge profile below the opposite end of the field plate arrangement.

Allowable Subject Matter

Claims 1-6, 8-13, 15 and 16 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Shouxiang Hu/
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